

ASIC CLOCK FLOOR PLANNING METHOD AND STRUCTURE

Abstract

A method of designing a clock tree in an integrated circuit combines steps of making a list of all clock sinks 110; positioning a temporary reference insertion point (TIP) 120; grouping the sinks together with structured clock buffers (SCBs) in a set of levels 140; and moving the SCBs to improve symmetry of the tree 150. The SCBs may be of several sizes and may be positioned horizontally 42 or vertically 45 and moved within limits 46 to permit the program to calculate a complete tree.